LISTING OF CLAIMS

This Listing of Claims will replace all prior versions and Listings of Claims in the application:

Claims 1-9. (Canceled).

10. (Original) A multi-clocked routing chip for use in an emulation system, the multi-clocked routing chip comprising:

a reconfigurable static routing circuit;

a first set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the first set of input/output circuitry is clocked by a first clock signal; and

a second set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the second set of input/output circuitry is clocked by a second clock signal different than the first clock signal.

11. (Previously Amended) The multi-clocked routing chip of claim 10, wherein the first and second sets of input/output circuitry each includes a plurality of one-to-n demultiplexers and a plurality of n-to-one multiplexers, where n is an integer greater than 1.

12. (Previously Amended) The multi-clocked routing chip of claim 10, further comprising a third set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the third set of input/output circuitry is clocked by a third clock signal different than the first and second clock signals.

Claims 13-22. (Canceled).

23. (Presently Amended) A ~~The~~ multi-clocked routing chip ~~of claim 10~~ for use in an emulation system, the multi-clocked routing chip comprising:

a reconfigurable static routing circuit;

a first set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the first set of input/output circuitry is clocked by a first clock signal; and

a second set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the second set of input/output circuitry is clocked by a second clock signal different than the first clock signal, wherein signals can be transferred out of the reconfigurable static routing circuit asynchronously to input of signals to the reconfigurable static routing circuit.

24. (New) The multi-clocked routing chip of claim 23, wherein the first and second sets of input/output circuitry each includes a plurality of one-to-n demultiplexers and a plurality of n-to-one multiplexers, where n is an integer greater than 1.

25. (New) The multi-clocked routing chip of claim 23, further comprising a third set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the third set of input/output circuitry is clocked by a third clock signal different than the first and second clock signals.